

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

Claim 1 (Previously presented): A process for forming vias in polymers with low dielectric constants, the process comprising the steps of:

- (a) providing a substrate layer;
- (b) forming a lower level layer on said substrate layer, selected from one or more of the group consisting of dielectric, metal and circuit devices;
- (c) forming a seed layer on top of said lower level layer;
- (d) forming a lower metal layer on said seed layer;
- (e) forming one or more pillars from a photoresist having top surfaces on said lower metal layer, defining photoresist pillars;
- (f) plating said photoresist pillars defining plated pillars;
- (g) removing the seed layer not under the lower level layer;
- (h) coating said one or more plated pillars and said seed layer with a low dielectric polymer;
- (i) curing said polymer;
- (j) exposing said top surfaces of said plated pillars; and
- (k) forming a metal layer to contact said exposed top surfaces of said plated pillars.

Claim 2 (Original): The process as recited in claim 1, wherein said coating step comprises coating with a low dielectric planarizing polymer.

Claim 3 (Original): The process as recited in claim 1, wherein said coating step comprises coating with a low dielectric, non-planarizing polymer and forming a planarizing coating over said non-planarizing polymer.

Claim 4 (Original): The process as recited in claim 1, further including the step of applying a dielectric layer to said plated pillars and bottom metal layer.

Claim 5 (Original): The process as recited in claim 4, wherein said step of applying a dielectric layer comprises applying SiO_2 .

Claim 6 (Original): The process as recited in claim 4, wherein said step of applying a dielectric layer comprises applying Si_3N_4 .

Claim 7 (Original): The process as recited in claim 1, wherein the step of coating comprises coating said one or more plated pillars and said lower metal layer with a silicon-based polymer.

Claim 8 (Original): The process as recited in claim 7, wherein the step of coating said one or more plated pillars and said lower metal layer comprises coating with benzocyclobutene.

Claim 9 (Original): The process as recited in claim 7, wherein the step of coating said one or more plated pillars and lower metal layer comprises coating with polynorbornene.

Claim 10 (Original): The process as recited in claim 1, wherein said step of forming said one or more plated pillars includes a step (k) of utilizing a photoresist with a re-entrant profile.

Claim 11 (Original): The process as recited in claim 10, wherein step (k) comprises utilizing a negative i-line resist.

Claim 12 (Original): The process as recited in claim 10, wherein step (k) comprises utilizing a NH_3 image reversal of a positive photoresist.

Claim 13 (Currently amended): A process for forming vias in polymers with low dielectric constants, the process comprising the steps of:

- (a) providing a substrate layer;
- (b) forming a lower level layer on said substrate, selected from one or more of the group consisting of dielectric, metal and a circuit device;
- (c) forming a bottom metal layer on said lower level layer;
- (d) forming one or more pillars from a photoresist on said lower metal layer;
- (e) coating said one or more pillars with a low dielectric polymer coating;

- (f) curing said polymer;
- (g) etching back said polymer to expose said one or more pillars;
- (h) removing said one or more pillars to form vias; and
- (i) forming a metal layer to contact said bottom metal layer on top of said polymer coating.

Claim 14 (Original): The process as recited in claim 13, further including the steps of:

- (j) forming a dielectric on top of said bottom metal layer and said lower level layer before said coating step; and
- (k) removing said dielectric layer from said bottom metal layer before said metal layer is formed on top of said polymer coating.

Claim 15 (Original): The process as recited in claim 14, wherein said step of forming a dielectric comprises forming a SiO₂ layer.

Claim 16 (Original): The process as recited in claim 14, wherein said step of forming a dielectric comprises forming a Si₃N₄ layer.

Claim 17 (Original): The process as recited in claim 13, wherein said coating step comprises coating with a low dielectric planarizing polymer.

Claim 18 (Original): The process as recited in claim 13, wherein said coating step comprises coating with a low dielectric, non-planarizing polymer and forming a planarizing coating over said non-planarizing polymer.

Claim 19 (Original): The process as recited in claim 13, wherein the step of coating comprises coating said one or more photoresist pillars with a silicon-based polymer.

Claim 20 (Original): The process as recited in claim 19, wherein the step of coating said one or more photoresist pillars comprises coating with benzocyclobutene.

Claim 21 (Original): The process as recited in claim 19, wherein the step of coating said one or more photoresist pillars comprises coating with polynorbornene.

Appl. No.: 10/016,693

Amdt. dated: 11/25/2003

Page 5

Reply to Office Action mailed July 25, 2003

Claim 22 (Original): The process as recited in claim 13 wherein the step of forming one or more pillars includes a step (l) of utilizing a photoresist with a re-entrant profile.

Claim 23 (Original): The process as recited in claim 22, wherein step (l) comprises utilizing a negative i-line resist.

Claim 24 (Original): The process as recited in claim 22, wherein step (l) comprises utilizing a NH_3 image reversal of a positive photoresist.